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| 13CS1102 | - | ADVANCED COMPUTER ARCHITECTURE |

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| Hours / Week | : | 4 |  | Sessional Marks | : | 40 |
| Credits | : | 4 |  | End Examination Marks | : | 60 |

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| **UNIT - I** |
| **Introduction**: Technological Advances, Performance Metrics and Evaluation. **Basics –** Pipelining, Caches, Virtual Memory and Paging |
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| **UNIT – II** |
| **Superscalar Processors:** From Scalar to Superscalar Processors, Instruction Pipeline of the DEC Alpha 21164, Register Renaming, Reorder Buffer and Reservation Stations, Pentium P6 Microarchitecture Overview, VLIW/EPIC Processors. |
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| **UNIT – III** |
| **Front-End:** Branch Prediction (The DEC Alpha 21264 Predictor), Instruction Fetching, Decoding, Register Renaming – a second look. **Back-End:** Instruction Issue and Scheduling, Memory-Accessing Instructions, Back-End Optimizations. |
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| **UNIT – IV** |
| **Cache Hierarchy**: Improving Access to L1 Caches, Hiding Memory Latencies, Design Issues for Large Higher-Level Caches, Main Memory**Multiprocessors:** Multiprocessor Organization, Cache Coherence, Synchronization, Relaxed Memory Models, Multimedia Instruction Set Extensions |
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| **UNIT – V** |
| **Multimedia and Chip Multiprocessing(CMP)**: Single-Processor Multithreading, General-Purpose Multithreaded Chip Multiprocessors, Special-Purpose Multithreaded Chip Multiprocessors, **Current Limitations and Future Challenges**: Power and Thermal Management, Technological Limitations: Wire Delays and Pipeline Depths, Challenges for Chip Multiprocessors. |
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| TEXT BOOKS |
| 1. Microprocessor Architecture: From Simple Pipelines to Chip Multiprocessors. By Jean-Loup Baer, Cambridge University Press.
2. Hennessy J L, Patterson D A, Computer Architecture: A Quantitative Approach, 4th edition, Morgan Kaufmann Publishers, 2007.
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| REFERENCE BOOKS |
| 1. Jordan H F, Alaghband G, Fundamentals of Parallel Processing, Prentice-Hall of India Ltd, 2003.
2. Dongarra J, Foster I, Fox G, Gropp W, Kennedy K, Torczon L, and White A, Morgan, Source Book of Parallel Computing, Kaufmann Publishers, 2003.
3. Hwang K, Advanced Computer Architecture: Parallelism, Scalability, Programmability, McGraw-Hill, 2001.
4. Sima D, Fountain T, Kacsuk P, Advanced Computer Architectures, Pearson Education, 1997.
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